REMARKS

This Amendment further addresses the outstanding final Office Action dated April 8, 2008. Applicants respectfully request favorable reconsideration of this application, as amended.

Claims 1-18 are pending. By this Amendment, Claims 1, 6 and 10 have been amended to more particularly recite the subject matter of Applicants' invention as discussed in detail below.

In the Office Action, Claims 1-18 were rejected under 35 U.S.C. § 103 over Takashi in combination with Kinoshita, Kitahara, and Moyer.

Without acceding to the rejections, Claim 1 has been amended to more particularly recite, *inter alia*, an isolation that is provided over a main surface of a semiconductor layer and that is constructed to have a depth that does not reach through to an insulator layer and also does not reach the support substrate layer, in which one of a portion and a whole of a plurality of bipolar transistors are surrounded by the insulator layer, the isolation, and an oxide film disposed within the isolation so as to not reach the support substrate layer. Support is provided, for example, at page 10, lines 8-11 and 21-27; page 11, lines 1-5; page 15, lines 25-29; and FIG. 8 of Applicants'

disclosure. It is apparent that the applied references do not teach or suggest this combination of features.

For example, the primary reference, Takashi, discloses a "P type substrate 1" and an "N type embedding layer 2." *See*, for example, Takashi, para. [0006]. It is apparent, however, that Takashi's "element isolating regions 4-1 and 4-2" do reach to the P-type substrate 1. *See* Takashi, FIG. 1(b). Therefore, Takashi does not teach or suggest an isolation that is provided over a main surface of a semiconductor layer and that is constructed to have a depth that does not reach through to an insulator layer and also does not reach the support substrate layer, in which one of a portion and a whole of a plurality of bipolar transistors are surrounded by the insulator layer, the isolation, and an oxide film disposed within the isolation so as to not reach the support substrate layer, as recited in Claim 1.

Furthermore, secondary reference Kinoshita discloses "a device separating isulative film 15, and an interlayer insulative film 16." *See* Kinoshita, col. 4, lines 54-55; and FIG. 8(b). However, Kinoshita is not understood as teaching or suggesting an isolation that is provided over a main surface of a semiconductor layer and that is constructed to have a depth that does not reach through to an insulator layer and also does not reach the support

substrate layer, in which one of a portion and a whole of a plurality of bipolar transistors are surrounded by the insulator layer, the isolation, and an oxide film disposed within the isolation so as to not reach the support substrate layer, as recited in Claim 1.

In addition, secondary reference Kitahara teaches an "element area 19, . . . defined by element isolation area 18 and oxide film 13 so that element area 19 may be electrically isolated from the other areas." *See* Kitahara, col. 4, lines 8-11p; and FIGS. 4 and 7. It is apparent, however, that Kitahara does not teach or suggest an isolation that is provided over a main surface of a semiconductor layer and that is constructed to have a depth that does not reach through to an insulator layer and also does not reach the support substrate layer, in which one of a portion and a whole of a plurality of bipolar transistors are surrounded by the insulator layer, the isolation, and an oxide film disposed within the isolation so as to not reach the support substrate layer, as recited in Claim 1.

Furthermore, secondary reference Moyer discloses oxide layers 98 and 102. *See* Moyer, col. 8, lines 24-27 and 38-42; and FIGS. 7 to 10a. However, Moyer is not seen as teaching an isolation at all, nor does the Office Action rely on Moyer for such teaching. It follows, of course,

that Moyer also does not teach or suggest an isolation that is provided over a main surface of a semiconductor layer and that is constructed to have a depth that does not reach through to an insulator layer and also does not reach the support substrate layer, in which one of a portion and a whole of a plurality of bipolar transistors are surrounded by the insulator layer, the isolation, and an oxide film disposed within the isolation so as to not reach the support substrate layer, as recited in Claim 1.

Therefore, Applicants respectfully submit that Claim 1 distinguishes patentably over the applied references.

In addition, Claim 6 has also been amended to more particularly recite, *inter alia*, an isolation that is provided over the main surface of a semiconductor layer and that is constructed to have a depth that does not reach through to an insulator layer and also does not reach a support substrate layer, in which one of a portion and a whole of a plurality of bipolar transistors are surrounded by the insulator layer, the isolation, and an oxide film disposed within the isolation so as to not reach the support substrate layer.

Furthermore, Claim 10 has been amended to more particularly recite, *inter alia*, a first isolation provided over the main surface of a semiconductor layer and that is

constructed to have a depth that does not reach through to an insulator layer and also does not reach a support substrate layer; a second isolation that is provided over the main surface of the semiconductor layer that is constructed to have a depth that does not reach through to the insulator layer and also does not reach the support substrate layer; that one of a portion and a whole of a plurality of first bipolar transistors are surrounded by the insulator layer, the first isolation in the first region, and an oxide film disposed within the first isolation so as to not reach the support substrate layer; and that one of a portion and a whole of a plurality of second bipolar transistors are surrounded by the insulator layer, the second isolation in the second region, and an oxide film disposed within the second isolation so as to not reach the support substrate layer.

Therefore, Applicants respectfully submit that Claims 6 and 10 also distinguish patentably over the applied references, for at least the reasons discussed above with respect to Claim 1.

Claims 2-5, 7-9, and 11-18 are also believed to be patentable due at least to their respective dependence from Claims 1, 6 and 10, as well as for the additional subject matter recited in Claims 2-5, 7-9, and 11-18.

Accordingly, a Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10036) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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